AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A plasma display panel, comprising:

a first substrate;

a second substrate facing the first substrate with a discharge space therebetween;

a sealing layer located between the first substrate and the second substrate;

at least one of a buffer layer or a dielectric layer formed between the first substrate and the sealing layer ~~to compensate the thermal stress of the first substrate and the sealing layer~~, wherein the at least one of the buffer layer or the dielectric layer includes the following composition: PbO at a ratio of 45% to 55%, B_2O_3 at a ratio of 10% to 20% and SiO_2 at a ratio of 15%-25%; and

~~an upper dielectric layer formed on the first substrate; and~~

a protective film formed on the ~~upper dielectric layer~~ at least one of the buffer layer or the dielectric layer.

2. (Cancelled)

3. (Currently Amended) The plasma display panel according to claim 1, wherein the buffer layer has a thermal expansion coefficient ~~of the buffer layer is~~ different from ~~the~~ a thermal expansion coefficient of the first substrate.

4. (Canceled)

5. (Currently Amended) The plasma display panel according to claim 1, wherein the buffer layer has a thermal expansion coefficient ~~of the buffer layer is~~ different from ~~the~~ a thermal expansion coefficient of the sealing layer.

6. (Canceled)

7. (Currently Amended) The plasma display panel according to claim 1, wherein the first substrate has a thermal expansion coefficient of ~~the first substrate is around~~ approximately $80X10^{-7}$~$95X10^{-7}$/°C.

8. (Currently Amended) The plasma display panel according to claim 1, wherein the sealing layer has a thermal expansion coefficient of ~~the sealing layer is around~~ approximately $65X10^{-7}$~$80X10^{-7}$/°C.

9. (Currently Amended) The plasma display panel according to claim 1, wherein the buffer layer has a thermal expansion coefficient of ~~the buffer layer is around~~ approximately $72X10^{-7}$~$86X10^{-7}$/°C.

10. (Canceled)

11. (Currently Amended) The plasma display panel according to claim 1, wherein ~~the upper~~ the plasma display panel includes both the buffer layer and the dielectric layer ~~dielectric layer is formed on the buffer layer and the protective film is formed on the upper dielectric layer~~ such that the buffer layer is provided between the first substrate and the ~~upper~~ dielectric layer and such that the ~~upper~~ dielectric layer is provided between the buffer layer and the protective film.

12. (Currently Amended) The plasma display panel according to claim 11, wherein the buffer layer is formed to be extended from the ~~upper~~ dielectric layer.

13. (Currently Amended) The plasma display panel according to claim [[1]] 11, wherein the buffer layer is separately formed of a different material from the ~~upper~~ dielectric layer.

14-25. (Canceled)

26. (Currently Amended) A plasma display panel, comprising:

a first substrate;

a second substrate arranged with respect to the first substrate such that a discharge space is provided therebetween;

a sealing layer between the first substrate and the second substrate; and

at least one of a buffer layer or a dielectric layer formed between the first substrate and the sealing layer ~~such that the buffer layer is provided only in an area between the first substrate and the sealing layer, the buffer layer to compensate thermal stress of the first substrate and the sealing layer~~, wherein the at least one of the buffer layer or the dielectric layer has a thermal expansion coefficient greater or equal to $72 \times 10^{-7}/°C$.

27. (Previously Presented) The plasma display according to claim 26, wherein the sealing layer extends in a longitudinal direction from a first end to a second end, the first end located proximal to the first substrate and the second end located proximal to the second substrate, the buffer layer provided only in the area between the first end of the sealing layer and the first substrate.

28. (Previously Presented) The plasma display according to claim 26, further comprising:

another sealing layer between the first substrate and the second substrate; and

another buffer layer formed between the first substrate and the another sealing layer such that the another buffer layer is provided only in another area between the first substrate and the another sealing layer, the another buffer layer to compensate thermal stress of the first substrate and the another sealing layer.

29. (Currently Amended) The plasma display panel according to claim 28, wherein the at least one of the buffer layer or the dielectric layer is the buffer layer, and the plasma display panel further comprising:

an upper dielectric layer formed on the first substrate between the buffer layer and the another buffer layer; and

a protective film formed on the upper dielectric layer.

30. (Currently Amended) The plasma display panel according to claim 26, wherein ~~a~~ the thermal expansion coefficient of the buffer layer is different from a thermal expansion coefficient of the first substrate.

31. (Currently Amended) The plasma display panel according to claim 26, wherein ~~a~~ the thermal expansion coefficient of the buffer layer is different from a thermal expansion coefficient of the sealing layer.

32. (Currently Amended) A plasma display comprising:

a first substrate;

a second substrate arranged with respect to the first substrate such that a discharge space is provided therebetween;

a sealing layer between the first substrate and the second substrate; and

at least one of a buffer layer or a dielectric layer provided on the first substrate and provided between the first substrate and the sealing layer ~~to compensate thermal stress of the first substrate and the sealing layer;~~

~~a dielectric layer on the buffer layer, the buffer layer being different than the dielectric layer~~, wherein the buffer layer has a thickness of 35μm to 50 μm between the sealing layer and the first substrate; and

a protective film on the at least one of the buffer layer or the dielectric ~~area such that the dielectric layer is between the buffer layer and the protective film and the buffer layer is between the first substrate and the dielectric~~ layer.

33. (Currently Amended) The plasma display panel according to claim 1, wherein the buffer layer is different than the ~~upper~~ dielectric layer.

34. (New) The plasma display panel according to claim 32, wherein the at least one of the buffer layer or the dielectric layer includes the following composition: PbO at a ratio of 45% to 55%, B_2O_3 at a ratio of 10% to 20% and SiO_2 at a ratio of 15% to 25%.

35. (New) The plasma display panel according to claim 32, wherein the at least one of the buffer layer or the dielectric layer has a thermal expansion coefficient greater or equal to $72x10^{-7}/°C$.

36. (New) The plasma display panel according to claim 32, wherein the at least one of the buffer layer or the dielectric layer is the buffer layer, and the dielectric layer is formed on the buffer layer such that the buffer layer is provided between the first substrate and the dielectric layer and such that the dielectric layer is provided between the buffer layer and the protective film.

37. (New) The plasma display panel according to claim 32, wherein the thickness of the buffer layer is 40μm to 50μm.

38. (New) The plasma display panel according to claim 26, wherein the at least one of the buffer layer or the dielectric layer has a thermal expansion coefficient greater or equal to $72x10^{-7}/°C$.

39. (New) The plasma display panel according to claim 26, wherein the at least one of the buffer layer or the dielectric layer include the following composition: PbO at a ratio of 45% to 55%, B_2O_3 at a ratio of 10% to 20% and SiO_2 at a ratio of 15% to 25%.